AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. *(Currently Amended)* ~~Apparatus~~An apparatus for processing data, said apparatus comprising:

a processing circuit for executing processing instructions from any of a plurality of instruction sets of processing instructions, each processing instruction being specified by an instruction address identifying that processing instruction's location in memory, the instruction address having a predetermined number of bits irrespective of the instruction set to which the associated processing instruction belongs, but a different number of most significant instruction address bits needing to be specified in the instruction address ~~for~~to uniquely identify processing instructions in different instruction sets; and

encoding logic for encoding ~~an~~at least one instruction address with an indication of the instruction set corresponding to that instruction to generate an n-bit encoded instruction address, the encoding logic being arranged to perform the encoding by performing a computation equivalent to removing any least significant bits not forming the instruction address bits needing to be specified, and extending the specified instruction address bits to n-bits by prepending a pattern of bits to the specified instruction address bits, the number of least significant bits removed and the pattern of bits prepended being dependent on the instruction set corresponding to that instruction.

2. *(Currently Amended)* ~~Apparatus~~The apparatus as claimed in Claim 1, wherein for each instruction set ~~the~~ a first pattern of bits prepended to the specified instruction address bits of an instruction address from that instruction set is related ~~by a shifted pattern with~~to ~~the~~ a second pattern of bits prepended to the specified instruction address bits of instruction addresses of different instruction sets by shifting the first pattern of bits.

3. *(Currently Amended)* ~~Apparatus~~The apparatus as claimed in Claim 1, wherein the encoding logic is arranged to perform the encoding by performing a computation equivalent to generating an intermediate value by pre-pending a predetermined pattern of bits to the specified instruction address bits of the instruction address and then selecting as the encoded instruction address n bits from the intermediate value.

4. *(Currently Amended)* ~~Apparatus~~The apparatus as claimed in Claim 1, further comprising compression logic for compressing a said encoded instruction address by performing a computation equivalent to partitioning that encoded instruction address into a plurality of x-bit sections, comparing each x-bit section with the corresponding x-bit section of a preceding encoded instruction address and outputting as a compressed encoded instruction address the most significant x-bit section that differs from the corresponding x-bit section of the preceding encoded instruction address, along with any less significant x-bit sections.

5. *(Currently Amended)* ~~Apparatus~~The apparatus as claimed in Claim 4, wherein the compression logic is arranged to associate with each x-bit section to be output from the

compression logic a flag to indicate whether that x-bit section is the last x-bit section being output as the compressed encoded instruction address.

6. *(Currently Amended)* ~~Apparatus~~The apparatus as claimed in Claim 5, wherein if a plurality of x-bit sections are to be output from the compression logic, the plurality of x-bit sections are output sequentially starting with the least significant x-bit section.

7. *(Currently Amended)* ~~Apparatus~~The apparatus as claimed in Claim 5, wherein the compression logic is further arranged to expand to y bits each x-bit section to be output from the compression logic, with the most significant y-x bits containing the flag.

8. *(Currently Amended)* ~~Apparatus~~The apparatus as claimed in Claim 7, wherein the flag is a single bit.

9. *(Currently Amended)* ~~Apparatus~~The apparatus as claimed in Claim 8, wherein y is 8 and x is 7.

10. *(Currently Amended)* ~~Apparatus~~The apparatus as claimed in Claim 1, wherein the encoding logic comprises an n-bit selector logic unit for receiving the intermediate value and an identifier signal identifying the instruction set associated with the instruction address contained within the intermediate value, the n-bit selector being arranged to output a predetermined n-bits of the intermediate value dependent on the identifier signal.

11. *(Currently Amended)* ~~Apparatus~~The apparatus as claimed in Claim 4, wherein the compression logic comprises a plurality of comparators, each comparator being arranged to receive a corresponding x-bit section of the encoded instruction address, and including temporary storage for storing the corresponding x-bit section of the preceding encoded instruction address, the comparator being arranged to compare the two x-bit sections and to generate a difference signal which is set when the two x-bit sections are different.

12. *(Currently Amended)* ~~Apparatus~~The apparatus as claimed in Claim 11, wherein the compression logic further comprises a flag generator logic arranged to generate for each x-bit section to be output from the compression logic a flag based on predetermined combinations of the difference signals generated by the plurality of comparators, such that a flag for a particular x-bit section is set if a more significant x-bit section is also to be output.

13. *(Currently Amended)* ~~Apparatus~~The apparatus as claimed in Claim 12, wherein the compression logic further comprises an output generator for generating the compressed encoded instruction address by pre-pending to each x-bit section to be output its corresponding flag, thereby generating as the output compressed encoded instruction address a sequence of y-bit sections.

14. *(Currently Amended)* ~~Apparatus~~The apparatus as claimed in Claim 4, wherein the encoding logic and compression logic are provided within a trace module used to trace activities of the processing circuit.

15. *(Currently Amended)* A tracing tool for a data processing apparatus, the data processing apparatus having a processing circuit for executing processing instructions from any of a plurality of instruction sets of processing instructions, each processing instruction being specified by an instruction address identifying that processing instruction's location in memory, the instruction address having a predetermined number of bits irrespective of the instruction set to which the associated processing instruction belongs, but a different number of most significant instruction address bits needing to be specified in the instruction address ~~for~~to uniquely identify processing instructions in different instruction sets, and the tracing tool comprising:

encoding logic for encoding ~~an~~at least one instruction address with an indication of the instruction set corresponding to that instruction to generate an n-bit encoded instruction address, the encoding logic being arranged to perform the encoding by performing a computation equivalent to removing any least significant bits not forming the instruction address bits needing to be specified, and extending the specified instruction address bits to n-bits by prepending a pattern of bits to the specified instruction address bits, the number of least significant bits removed and the pattern of bits prepended being dependent on the instruction set corresponding to that instruction.

16. *(Currently Amended)* ~~A~~The tracing tool as claimed in Claim 15, further comprising compression logic for compressing an encoded instruction address by performing a computation equivalent to partitioning the encoded instruction address into a plurality of x-bit sections, comparing each x-bit section with the corresponding x-bit section of a preceding encoded instruction address and outputting as the compressed encoded instruction address the most

significant x-bit section that differs from the corresponding x-bit section of the preceding encoded instruction address, along with any less significant x-bit sections.

17. *(Currently Amended)* A method of storing instruction set information, a processing circuit being arranged to execute processing instructions from any of a plurality of instruction sets of processing instructions, each processing instruction being specified by an instruction address identifying that processing instruction's location in memory, the instruction address having a predetermined number of bits irrespective of the instruction set to which the associated processing instruction belongs, but a different number of most significant instruction address bits needing to be specified in the instruction address ~~for~~to uniquely identify processing instructions in different instruction sets, the method comprising the steps of:

encoding logic encoding ~~an~~at least one instruction address with an indication of the instruction set corresponding to that instruction to generate an n-bit encoded instruction address, by performing a computation equivalent to:

the encoding logic removing any least significant bits not forming the instruction address bits needing to be specified, and

the encoding logic extending the specified instruction address bits to n-bits by prepending a pattern of bits to the specified instruction address bits, the number of least significant bits removed and the pattern of bits prepended being dependent on the instruction set corresponding to that instruction.

18. *(Currently Amended)* ~~A~~The method as claimed in Claim 17, further comprising the step of compressing a said encoded instruction address by performing a computation equivalent to:

partitioning the encoded instruction address into a plurality of x-bit sections;

comparing each x-bit section with the corresponding x-bit section of a preceding encoded instruction address; and

outputting as the compressed encoded instruction address the most significant x-bit section that differs from the corresponding x-bit section of the preceding encoded instruction address, along with any less significant x-bit sections.

19. *(Currently Amended)* ~~A~~The method ~~of decompressing a compressed encoded instruction address generated in accordance with the method of~~as claimed in Claim 18, further comprising decompressing the compressed encoded instruction address by performing a computation equivalent to:

determining the number of x-bit sections forming the compressed encoded instruction address; and

extending as necessary the compressed encoded instruction address to n-bits by incorporating additional x-bit sections obtained from corresponding x-bit sections of a preceding encoded instruction address, thereby producing the encoded instruction address.

20. *(Currently Amended)* ~~A~~The method as claimed in Claim 19, further comprising the step of decoding the encoded instruction address by performing a computation equivalent to determining from the predetermined pattern of bits the instruction set to which the instruction

address relates, and removing the predetermined pattern of bits to yield the specified instruction address bits.

21. *(Currently Amended)* A computer ~~program product~~readable medium carrying a computer program for controlling an apparatus in accordance with the method of claim 17.

22. *(New)* The apparatus as claimed in claim 1, wherein the encoding logic is provided within a trace module used to trace activities of the processing circuit.